RTμL COMPOSITE DATA SHEET

INDUSTRIAL MICROLOGIC® INTEGRATED CIRCUITS

OPERATING TEMPERATURE RANGE: 0°C to +70°C (METAL PACKAGE)
15°C to 55°C (EPOXY)

GENERAL DESCRIPTION — The Fairchild Industrial Resistor-Transistor Micrologic® (RTμL) integrated circuit family consists of a number of medium and low power compatible integrated circuits made up by resistor-transistor logic and capable of performing logic functions for use in digital electronic equipment.

The elements of this family are manufactured using the familiar Fairchild Planar* epitaxial process by which all the individual transistors and resistors are diffused into a single silicon wafer, thus assuring a high degree of reliability.

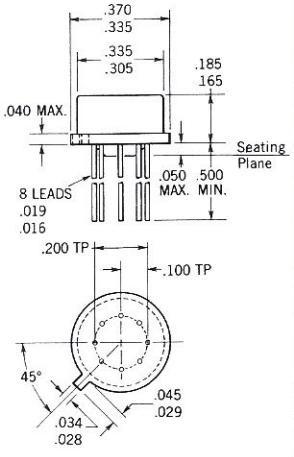
*Planar is a patented Fairchild process.

Some of the important features of the RTμL integrated circuit family are the following:

- Guaranteed operation over the specified temperature range.
- System operates with one power supply (3.6 V±10%).
- Trade-off between fan-out and temperature (permitted).
- RTL uses positive NOR or negative NAND logic.
- High noise immunity — 300 mV.
- Very low propagation delays — typical 12 nanoseconds for medium power gate and 40 nanoseconds for low power gate.
- Power dissipation of typically 2mW per gate for the low power elements.
- Low cost.
- Medium power buffer 9900, dual two-input gate 9914 and JK flip-flop9923 available in epoxy for additional cost advantages.
- Mixing medium and low power elements optimizes fan-out and power dissipation.
- Application briefs, notes and thorough individual data sheets available.

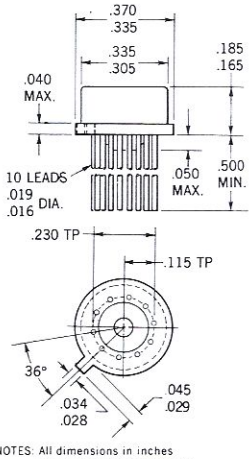
PHYSICAL DIMENSIONS (TO-5 TYPES)

TO-99
(8 pin package)



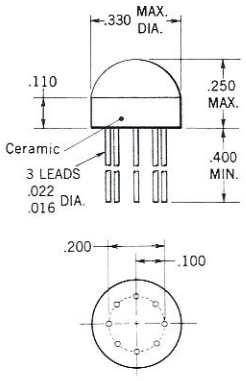
NOTES: All dimensions in inches
Dimensions as per latest J-10 committee
Leads are gold-plated kovar
Weight is 1.12 grams

TO-100
(10 pin package)



NOTES: All dimensions in inches
Leads are gold-plated kovar
Lead No. 1 internally connected to case
Package weight is 1.32 grams

EPOXY PACKAGE
(similar to TO-5)



NOTES: All dimensions in inches
Leads are gold-plated nickel

PURCHASING INFORMATION

Purchasing Agent please note:

To order part, the following numbering system should be used to expedite handling. The complete number will be a nine-digit number with the designations as follows:

A B C D E F G H I

A = U for all elements

BC = 5B for 8-pin (TO-99) pkg.
= 5F for 10-pin (TO-100) pkg.
= 8A for 8-pin epoxy

DEFG = The four-digit number denoting the specific element desired

H = 2 for all elements

I = 9 for 0°C to 70°C for metal packages
= 8 for 15°C to 55°C epoxy pkg.

Note: All elements are available in a metal TO-5 type package, but not necessarily in epoxy. Consult your sales representative for details.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

COPYRIGHT FAIRCHILD SEMICONDUCTOR 1967 • PRINTED IN U.S.A. 2320-160-17 10M
MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 291877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

LOADING RULES

Industrial Resistor-Transistor Micrologic® (RTμL) integrated circuits consist of low and medium power devices. The primary difference between a low and a medium power element lies in the values of the base and collector resistors associated with each element. The medium power elements have base and collector resistors of 450 Ω and 640 Ω typical, whereas the low power elements have typical base and collector resistors of 1.5 kΩ and 3.6 kΩ respectively.

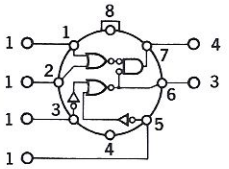
As a result of these differences in resistance values, the input load and output drive factors (maximum input current and minimum output available current) are higher for the medium, and lower for the low power elements.

For purposes of simplification, all input load and output drive factors have been normalized using as a basis the current required to turn on a low-power gate transistor. As a result of this normalization, the input load factor of the 9914 element is 3 and the input load factor of the 9910 element is 1, thus, the 9914 requires three times as much input current. For the output drive factors, the 9910 has an output drive factor four times less than that of the 9914.

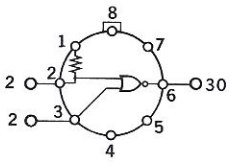
The number of elements (bases) that may be driven by an output terminal may consist of any combination of low and medium power elements as long as the sum of all the input load factors does not exceed the output drive factor of the driving element.

LOADING CHART

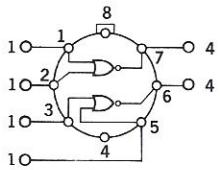
LOW POWER ELEMENTS:



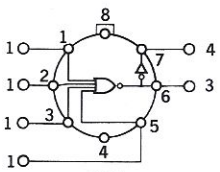
9908



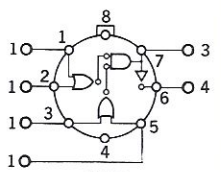
9909



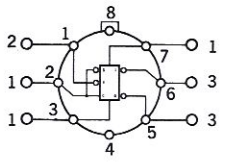
9910



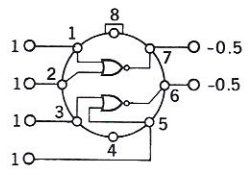
9911



9912

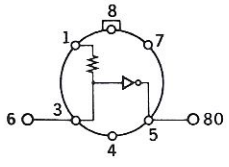


9913

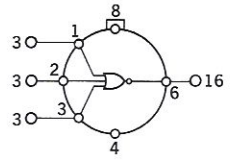


9921

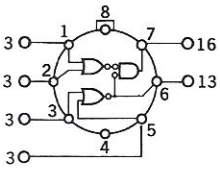
MEDIUM POWER ELEMENTS:



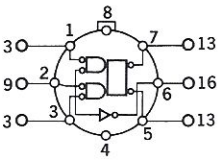
9900



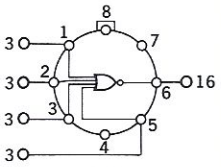
9903



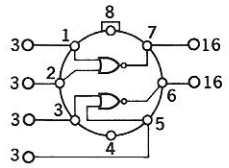
9904



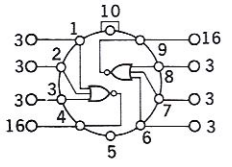
9905



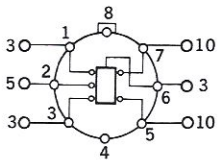
9907



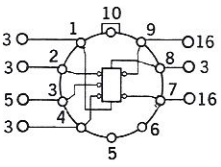
9914



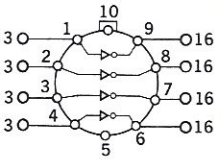
9915



9923



9926



9927

PARALLELING AND OTHER RULES:

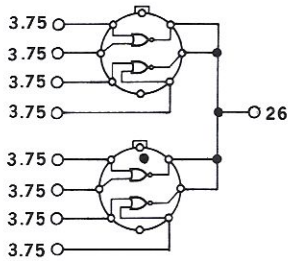
1. All unused input pins should be grounded.

2. On all 8-pin lead devices, V_{CC} is connected to pin 8 and pin 4 is grounded. On 10-pin lead devices, pins 10 and 5 are V_{CC} and Ground pins respectively.

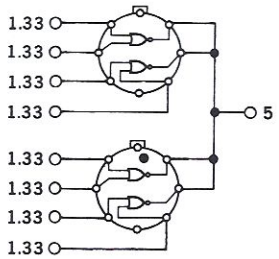
3. For each medium power gate output terminal tied to another medium power gate output terminal (and V_{CC} open on all gates but one) the output drive factor should be reduced by 2 loads.

4. For each low-power gate output terminal tied to another low power gate output terminal (and V_{CC} open on all gates but one) the output drive factor should be reduced by one load.

5. By increasing the input load requirement by 0.75 load for medium power and 0.33 for low power to cover any reduction in base-emitter impedance, any number of gates may be placed in parallel as shown below:



PARALLELING MEDIUM POWER ELEMENTS

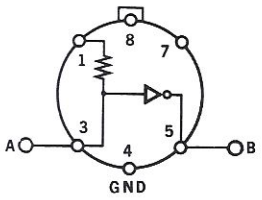


PARALLELING LOW POWER ELEMENTS

● = NO V_{CC} CONNECTED

9900 MEDIUM POWER BUFFER*

The Buffer element is a low-impedance inverting driver circuit. Because of its very low source impedance the element can supply substantially more output current than the basic circuit. As a consequence, the Buffer element is valuable in driving heavily loaded circuits or minimizing rise-time deterioration due to capacitive loading. A resistor is internally connected to the Buffer element input which may be returned to the supply voltage if capacitive coupling is desired. Typical applications of this type connection are astable and monostable multivibrators, and for the differentiation of pulses.

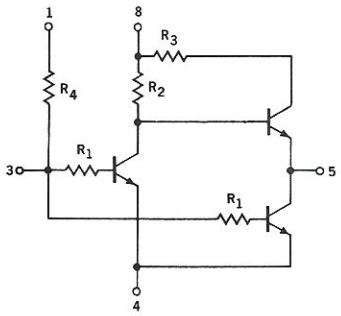


FUNCTIONS

POSITIVE LOGIC:
$B = \overline{A}$

NEGATIVE LOGIC:
$B = \overline{\overline{A}}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

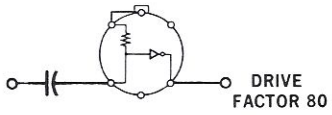
$R_1 = 450\Omega$
$R_2 = 1000\Omega$
$R_3 = 100\Omega$
$R_4 = 1000\Omega$

LOADING RULES

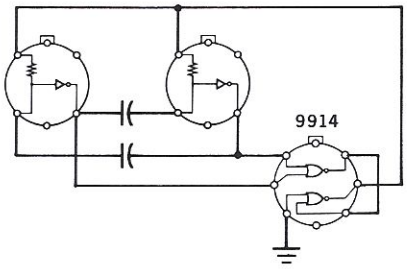
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
3	6	5	80

Note: For more information on loading rules and for parallel combination of elements, see page 2.

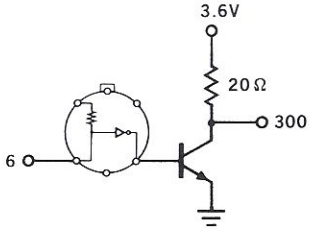
TYPICAL APPLICATIONS



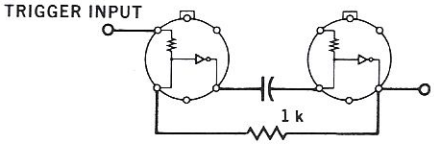
ONE SHOT MULTIVIBRATOR



ASTABLE MULTIVIBRATOR



HIGH FAN-OUT EXTENSION



MONOSTABLE CIRCUIT

* This element also available in the epoxy package.

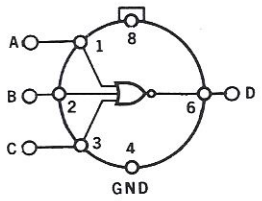
9903 MEDIUM POWER THREE INPUT GATE

The Gate element is a three-input resistor-transistor-logic circuit, one of four similar-basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic function through the exclusive use of gate elements. Individual gate elements may be paralleled to increase the number of inputs to a single output node (subject to loading rules), or combined with other Micrologic® integrated circuits to augment their logic functions.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



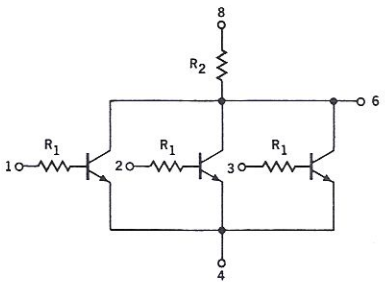
FUNCTIONS

POSITIVE LOGIC: $D = \overline{A + B + C}$

NEGATIVE LOGIC: $D = \overline{A}\,\overline{B}\,\overline{C} = \overline{A} + \overline{B} + \overline{C}$

Note: Pins 5 and 7 omitted.

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 650\Omega$

TRUTH TABLE

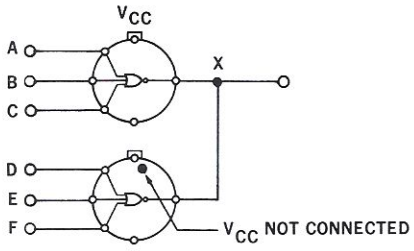
A	B	C	D
H	H	H	L
H	H	L	L
H	L	H	L
H	L	L	L
L	H	H	L
L	H	L	L
L	L	H	L
L	L	L	H

LOADING RULES

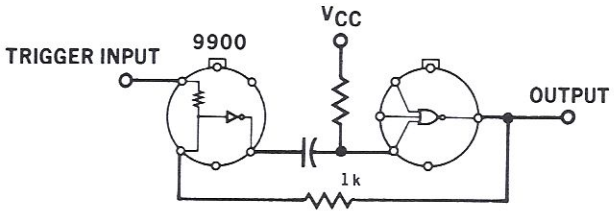
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3		
3	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



SIX INPUT GATE



MONOSTABLE CIRCUIT

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F}$

NEGATIVE LOGIC:
$\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F}$

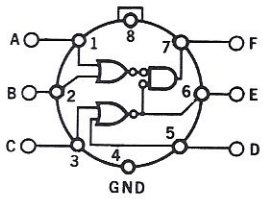
9904 MEDIUM POWER HALF ADDER

The Half-Adder element is a multipurpose combination of three basic circuits. The configuration is well-suited as a complete half-adder, an exclusive OR gate, or any other similar logic construction. Output No. 7 is a noninverting function of the four inputs, whereas output No. 6 may be considered as either a NAND or a NOR gate.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC: $E = \overline{C + D}$, $F = (A + B)(C + D)$

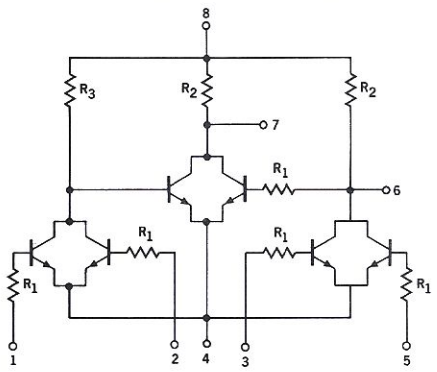
NEGATIVE LOGIC: $E = \overline{C}\,\overline{D}$, $F = AB + CD$

IF $C = \overline{A}$ and $D = \overline{B}$

POSITIVE LOGIC: $E = AB$, $F = A\overline{B} + \overline{A}B$

NEGATIVE LOGIC: $E = A + B$, $F = AB + \overline{C}\,\overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$
$R_3 = 800\Omega$

TRUTH TABLE

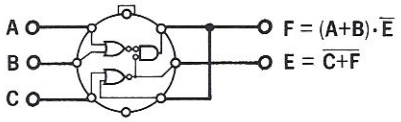
INPUTS				OUTPUTS	
1	2	3	5	7	6
H	H	H	H	H	L
L	H	H	H	H	L
H	L	H	H	H	L
H	H	L	H	H	L
H	H	H	L	H	L
L	L	H	H	L	L
L	H	L	H	H	L
L	H	H	L	H	L
H	L	L	H	H	L
H	L	H	L	H	L
H	H	L	L	L	H
L	L	L	H	L	L
L	H	L	L	L	H
L	L	H	L	L	L
H	L	L	L	L	H
L	L	L	L	L	H

LOADING RULES

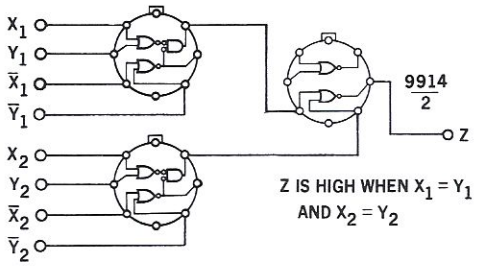
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3	7	13
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



GATED FLIP - FLOP



PARALLEL COMPARISON

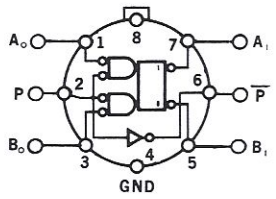
9905 MEDIUM POWER HALF SHIFT REGISTER

The Half Shift Register element is a gated input storage element composed of five basic gate circuits. Internal cross-connection of the two output gate circuits provides memory. The input gating signal is applied to the remaining three gate circuits. Two of these control the logic inputs, while the third provides the complement of the gating signal at an output pin. Because of the two cascaded internal logic levels, the unit changes state in response to near-ground input signals. Consequently, from a terminal standpoint, the unit should be regarded as requiring NAND input logic levels. Concurrent near-ground signals at all three inputs will cause near-ground signals at both outputs.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

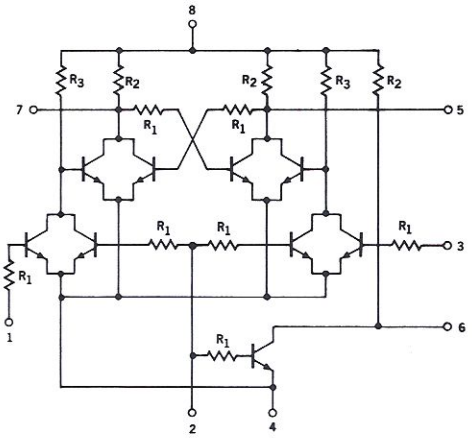


FUNCTIONS

POSITIVE LOGIC: $A_I = \overline{B_I}\,(A_0 + P)$, $B_I = \overline{A_I}\,(B_0 + P)$

NEGATIVE LOGIC: $A_I = \overline{B_I} + A_0P$, $B_I = \overline{A_I} + B_0P$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$
$R_3 = 800\Omega$

TRUTH TABLE

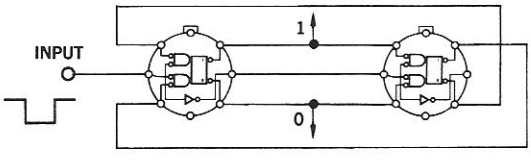
INPUT			OUTPUT	
A_0	P	B_0	A_I	B_I
H	H	H	H	L
H	H	L	H	L
H	L	H	H	L
H	L	L	H	L
L	H	H	L	H
L	H	L	L	H
L	L	H	L	H
L	L	L	L	L

LOADING RULES

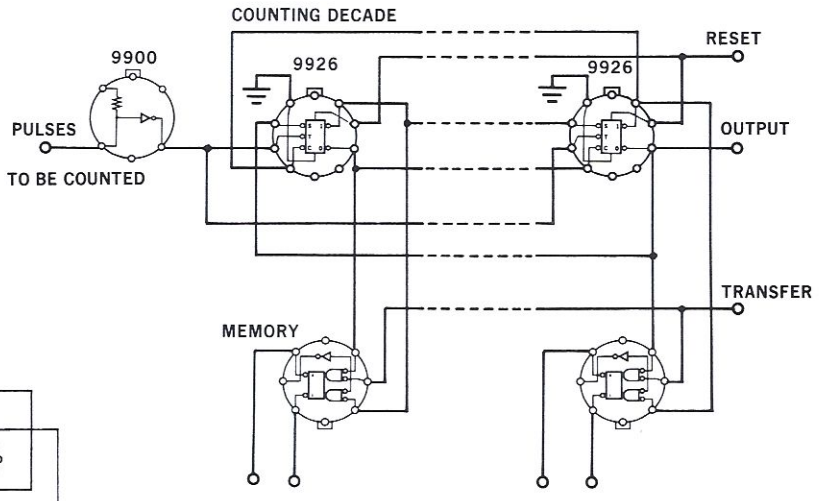
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	3	5	13
2	9	6	16
3	3	7	13

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



COMPLEMENTARY FLIP-FLOP



COUNTING DECADE WITH MEMORY

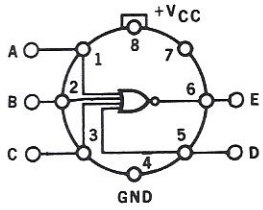
9907 MEDIUM POWER FOUR INPUT GATE

The Four-Input Gate element is a four-input resistor-transistor-logic circuit, one of four similar NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of four-input gate elements. Individual four-input gate elements may be paralleled to increase the number of inputs to a single output node (subject to loading rules), or combined with other Micrologic® integrated circuits to augment their logic functions. This element performs the AND and exclusive OR function. It is also used to select one of two data streams under control of a single gate signal.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

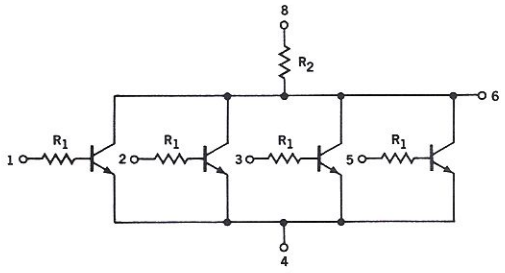


FUNCTIONS

POSITIVE LOGIC: $E = \overline{A + B + C + D} = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$

NEGATIVE LOGIC: $E = \overline{A\,B\,C\,D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

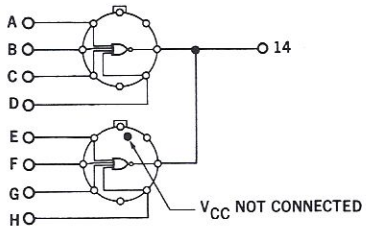
INPUTS				OUTPUT
A	B	C	D	E
H	H	H	H	L
H	H	H	L	L
H	H	L	H	L
H	H	L	L	L
H	L	H	H	L
H	L	H	L	L
H	L	L	H	L
H	L	L	L	L
L	H	H	H	L
L	H	H	L	L
L	H	L	H	L
L	H	L	L	L
L	L	H	H	L
L	L	H	L	L
L	L	L	H	L
L	L	L	L	H

LOADING RULES

INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3		
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



EIGHT INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F + G + H} = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F}\,\overline{G}\,\overline{H}$

NEGATIVE LOGIC:
$\overline{A\,B\,C\,D\,E\,F\,G\,H} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

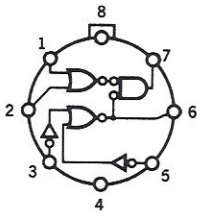
9908 LOW POWER ADDER

This element performs the AND and exclusive OR function. It is also used to select one of two data streams under control of a single gate signal.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

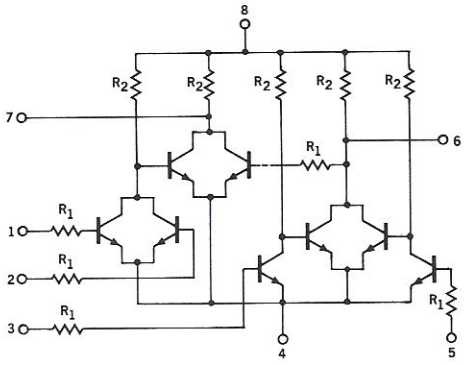


FUNCTIONS

POSITIVE LOGIC:
$6 = (\overline{3} + \overline{5}) = 3 \cdot 5$
$7 = (1 + 2)(\overline{3} + \overline{5})$

NEGATIVE LOGIC:
$6 = (\overline{3} \cdot \overline{5}) = 3 + 5$
$7 = 1 \cdot 2 + \overline{3} \cdot \overline{5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

I, Output "6"

3	5	6
L	L	L
L	H	L
H	L	L
H	H	H

II, Output "7"

1	2	6	7
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

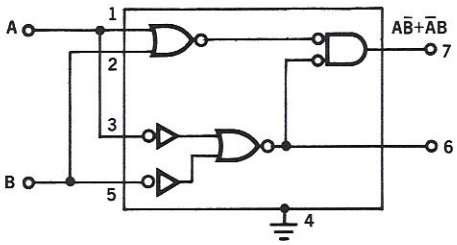
LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	3
2	1	7	4
3	1		
5	1		

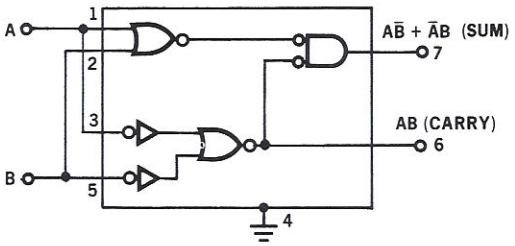
* For loading rule explanations see page 10.

Note: For more information on loading rules and for parallel combination of elements, see page 2.

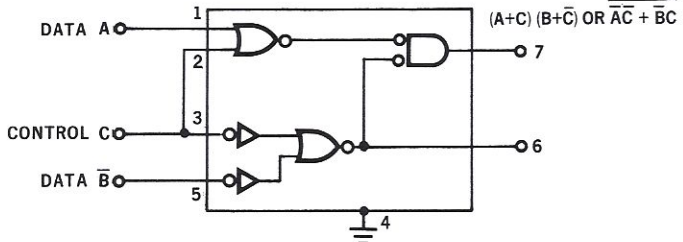
TYPICAL APPLICATIONS (POSITIVE LOGIC)



EXCLUSIVE OR GATE



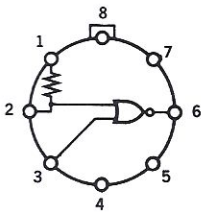
HALF ADDER



DATA STREAM SWITCH

9909 LOW POWER BUFFER

This element is a low-output impedance, two-input inverting driver. It can supply substantially more output current than the basic circuit to provide higher fan-out or drive capacitive loads. A resistor is connected internally to one of the inputs which may be returned to the supply voltage if capacitive coupling is desired.

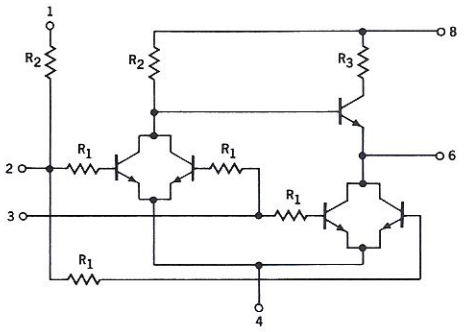


FUNCTIONS

POSITIVE LOGIC:
$6 = \overline{2 + 3}$

NEGATIVE LOGIC:
$6 = \overline{2 \cdot 3}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

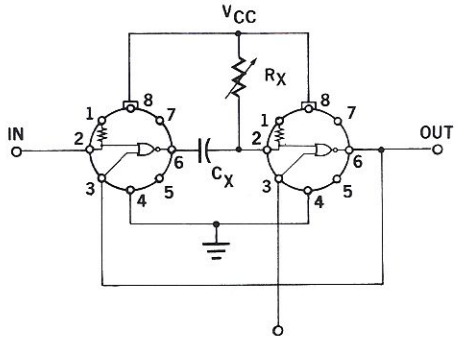
$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$
$R_3 = 100\Omega$

LOADING RULES

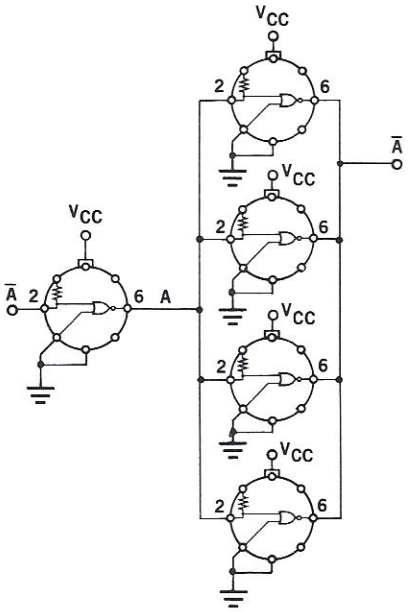
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
2 3	2 2	6	30

Note: For more information on loading rules and for parallel combination of elements, see page 2.

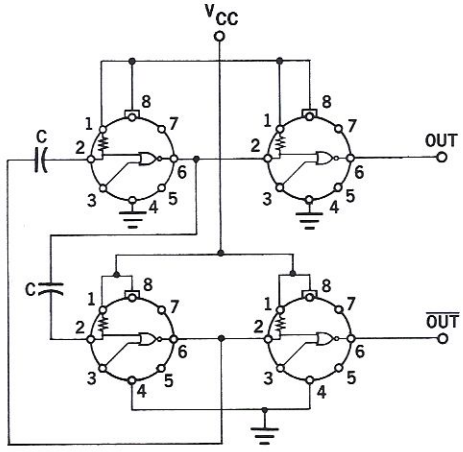
TYPICAL APPLICATIONS



ONE SHOT MULTIVIBRATOR



PARALLEL PULSE DRIVER



FOUR BUFFERS CONNECTED AS FREE RUNNING MULTIVIBRATOR

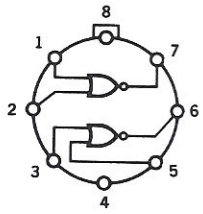
9910 LOW POWER DUAL GATE

This element can be used on a NOR gate, Double Inverter RS flip-flop or as a pair of Inverters. It can also be used with the gate expander to increase its fan-in capacity.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

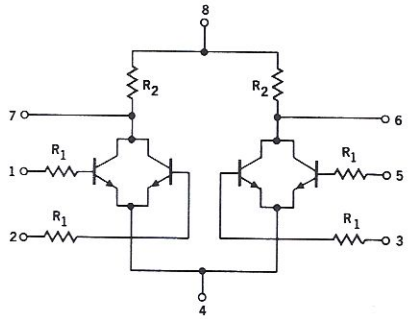


FUNCTIONS

POSITIVE LOGIC:
$7 = \overline{1 + 2}$
$6 = \overline{3 + 5}$

NEGATIVE LOGIC:
$7 = \overline{1 \cdot 2}$
$6 = \overline{3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

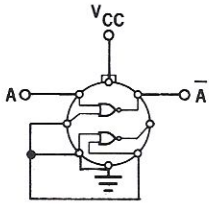
OUTPUT 7			OUTPUT 6		
1	2	7	3	5	6
L	L	H	L	L	H
L	H	L	L	H	L
H	L	L	H	L	L
H	H	L	H	H	L

LOADING RULES

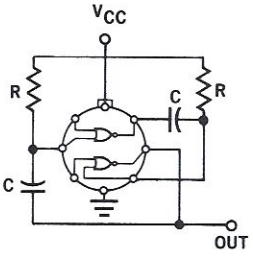
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	4
2	1	7	4
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

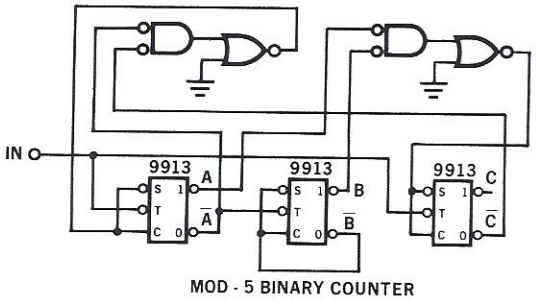
TYPICAL APPLICATIONS



SIMPLE INVERTER

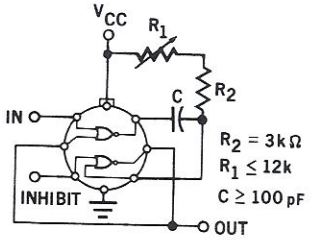


SINGLE DUAL GATE AS
FREE-RUNNING MULTIVIBRATOR



MOD - 5 BINARY COUNTER

Function: To count to a Modulo of 5 using a 1-2-4 code, or to divide an input frequency by a factor of 5.



SINGLE DUAL GATE USED AS
A ONE-SHOT MULTIVIBRATOR

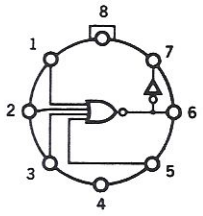
9911 LOW POWER DUAL GATE WITH INVERTER

This element is a general purpose four-input gate with inverter for NOR, OR functions and can also be used as an amplifier-inverter.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC:

$7 = 1 + 2 + 3 + 5$

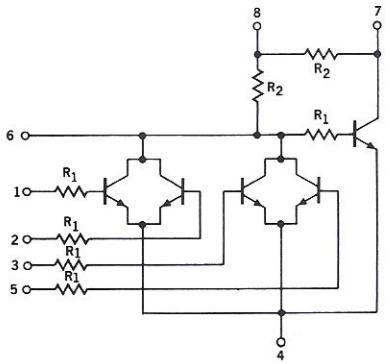
$6 = \overline{1 + 2 + 3 + 5}$

NEGATIVE LOGIC:

$7 = 1 \cdot 2 \cdot 3 \cdot 5$

$6 = \overline{1 \cdot 2 \cdot 3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

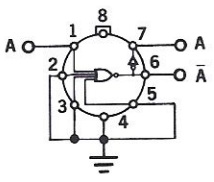
1	2	3	5	6	7
L	L	L	L	H	L
L	L	L	H	L	H
L	L	H	L	L	H
L	L	H	H	L	H
L	H	L	L	L	H
L	H	L	H	L	H
L	H	H	L	L	H
L	H	H	H	L	H
H	L	L	L	L	H
H	L	L	H	L	H
H	L	H	L	L	H
H	L	H	H	L	H
H	H	L	L	L	H
H	H	L	H	L	H
H	H	H	L	L	H
H	H	H	H	L	H

LOADING RULES

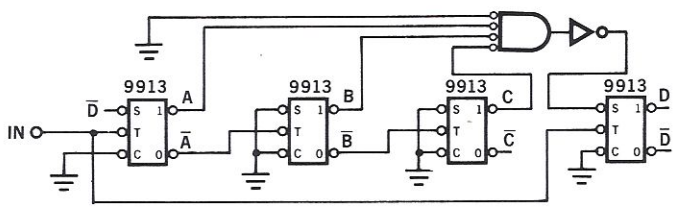
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	3
2	1	7	4
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



CONNECTED AS INVERTER-AMPLIFIER



MODULO 9 BINARY COUNTER

Function: To count to a Modulo of 9 using 1-2-4-8 code, or to divide an input frequency by a factor of 9.

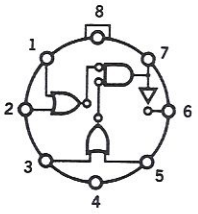
9912 LOW POWER HALF ADDER

This element is a multipurpose combination of three basic circuits that can be used as a complete half adder, an exclusive OR gate, gated-set flip-flop or any other similar logic construction.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC:

$7 = (1 + 2) \cdot (3 + 5)$

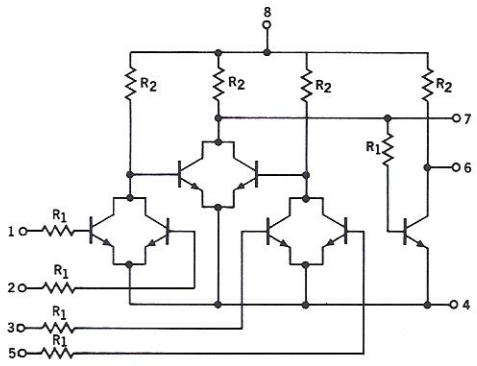
$6 = \overline{1} \cdot \overline{2} + \overline{3} \cdot \overline{5}$

NEGATIVE LOGIC:

$7 = 1 \cdot 2 + 3 \cdot 5$

$6 = (\overline{1} + \overline{2}) \cdot (\overline{3} + \overline{3})$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

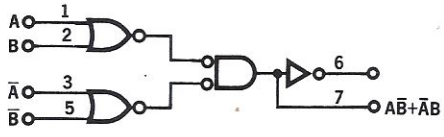
1	2	3	5	6	7
L	L	L	L	H	L
L	L	L	H	H	L
L	L	H	L	H	L
L	L	H	H	H	L
L	H	L	L	H	L
L	H	L	H	L	H
L	H	H	L	L	H
L	H	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	L	H	L	L	H
H	L	H	H	L	H
H	H	L	L	H	L
H	H	L	H	L	H
H	H	H	L	L	H
H	H	H	H	L	H

LOADING RULES

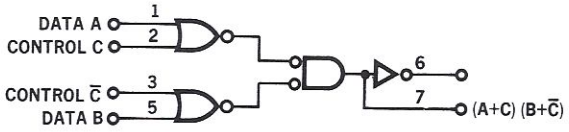
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	4
2	1	7	3
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

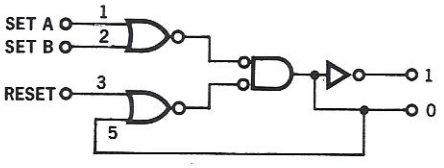
TYPICAL APPLICATIONS (POSITIVE LOGIC)



EXCLUSIVE OR GATE OR HALF ADDER



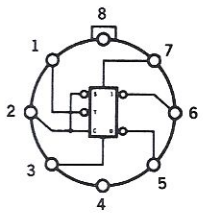
DATA STREAM SWITCH



GATED R-S FLIP-FLOP

9913 LOW POWER TYPE D FLIP FLOP

The 9913 is a gated flip-flop very suitable for shift registers and control circuitry. The state of the input at pin 2 is stored in the element when the input at pin 1 changes from logical "1" to logical "0." The element can be reset only when pin 1 is maintained at a logical "1" during the time that pin 7 undergoes a change from a logical "0" to a logical "1."

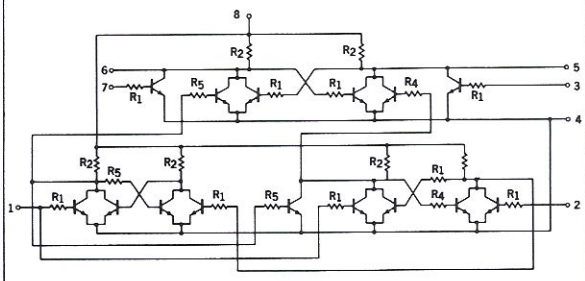


FUNCTIONS

DIRECT INPUTS[1]				GATED INPUT[3] t = n		t = n + 1
3	7	6	5	2	6	5
L	L	NC	NC[2]	H	H	L
L	H	L	H	L	L	H
H	L	H	L			
H	H	L	L			

(1) Pin 1 must be high.
(2) NC = No change.
(3) Pins 3 and 7 must be low.

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$
$R_4 = 180\Omega$
$R_5 = 480\Omega$

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

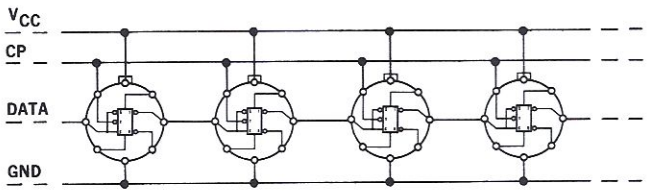
NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

LOADING RULES

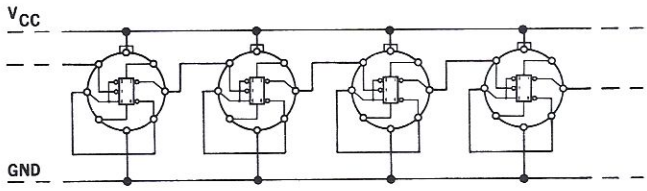
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	2	5	3
2	1	6	3
3	1		
7	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

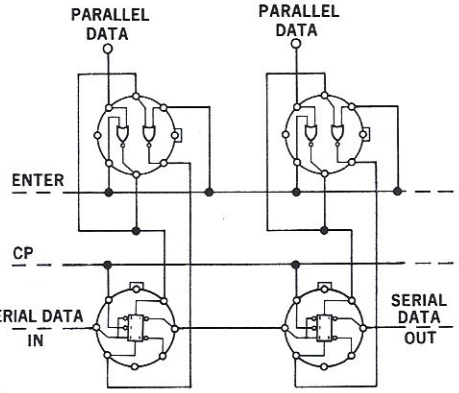
TYPICAL APPLICATIONS



SHIFT REGISTER STAGES USING TYPE D FLIP-FLOP



BINARY RIPPLE CARRY COUNTER STAGES USING TYPE D FLIP-FLOP



METHOD OF PARALLEL ENTRY OF DATA INTO SHIFT REGISTER
V_{CC} AND GROUND CONNECTIONS ARE NOT SHOWN

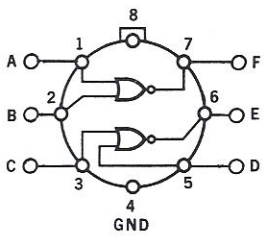
9914 MEDIUM POWER DUAL TWO INPUT GATE*

The Dual Two-Input Gate element is a dual combination of two-input resistor-transistor-logic circuits, one of four similar basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of dual two-input gate elements. In addition to the applications of other gate-type elements, the dual two-input gate element circuits may be cross-connected to form a flip-flop, or in tandem to form noninverting gates.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

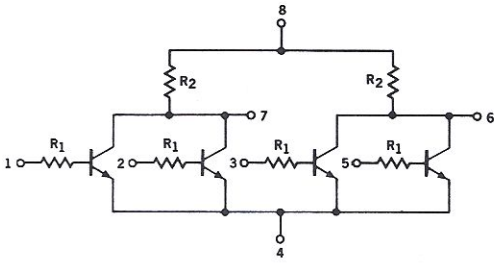


FUNCTIONS

POSITIVE LOGIC:
$F = \overline{A + B} = \overline{A}\,\overline{B}$
$E = \overline{C + D} = \overline{C}\,\overline{D}$

NEGATIVE LOGIC:
$F = \overline{A}\,\overline{B} = \overline{A} + \overline{B}$
$E = \overline{C}\,\overline{D} = \overline{C} + \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES
$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

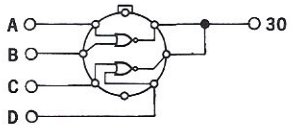
A	B	F
H	H	L
H	L	L
L	H	L
L	L	H

LOADING RULES

INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	6	16
2	3	7	16
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

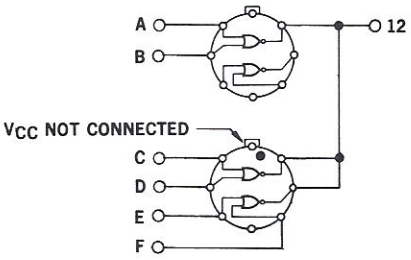
TYPICAL APPLICATIONS



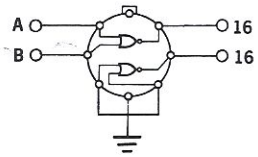
FOUR INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

NEGATIVE LOGIC:
$\overline{A\,B\,C\,D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$



SIX INPUT GATE



TWO INPUT GATE

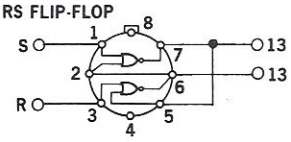
POSITIVE LOGIC:
$\overline{A + B} = \overline{A} \cdot \overline{B}$

NEGATIVE LOGIC:
$\overline{A} \cdot \overline{B} = \overline{A} + \overline{B}$

PIN NUMBERS			
INPUT		OUTPUT	
1	3	6	7
L	L	NC	NC
L	H	L	H
H	L	H	L
H	H	NOT ALLOWED	

NC = No change.

RS FLIP-FLOP



* This element also available in the epoxy package.

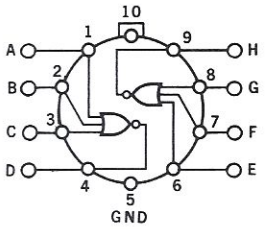
9915 MEDIUM POWER DUAL THREE INPUT GATE

The Dual Three-Input Gate element is a dual combination of three-input resistor-transistor-logic circuits, one of four similar basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of dual three-input gate elements. In addition to the applications of other gate-type elements, the dual three-input gate element circuits may be cross-connected to form a flip-flop with 2 set and 2 reset inputs, or in tandem to form non-inverting gates.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

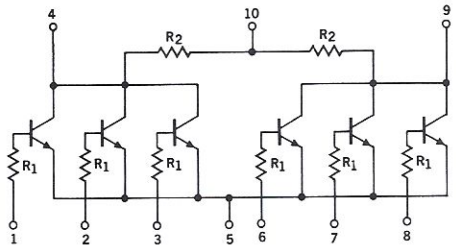


FUNCTIONS

POSITIVE LOGIC:
$D = \overline{A + B + C} = \overline{A}\,\overline{B}\,\overline{C}$
$H = \overline{E + F + G} = \overline{E}\,\overline{F}\,\overline{G}$

NEGATIVE LOGIC:
$D = \overline{A\,B\,C} = \overline{A} + \overline{B} + \overline{C}$
$H = \overline{E\,F\,G} = \overline{E} + \overline{F} + \overline{G}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

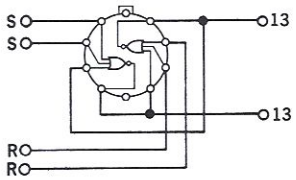
A	B	C	D
H	H	H	L
H	H	L	L
H	L	H	L
H	L	L	L
L	H	H	L
L	H	L	L
L	L	H	L
L	L	L	H

LOADING RULES

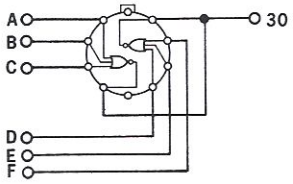
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	4	16
2	3	9	16
3	3		
6	3		
7	3		
8	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



RS FLIP-FLOP



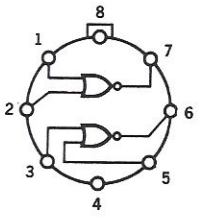
SIX INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F}$

NEGATIVE LOGIC:
$\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F}$

9921 LOW POWER GATE EXPANDER

This element is a double gate without the node resistors. Its output terminals may be connected in parallel to those of the 9910 or 9911 elements to increase the fan-in capability of the circuit. Pin 8 of the element must always be connected to V_{CC}.



FUNCTIONS

POSITIVE LOGIC:

$7 = \overline{1 + 2}$

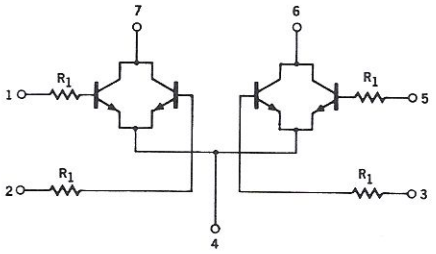
$6 = \overline{3 + 5}$

NEGATIVE LOGIC:

$7 = \overline{1 \cdot 2}$

$6 = \overline{3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

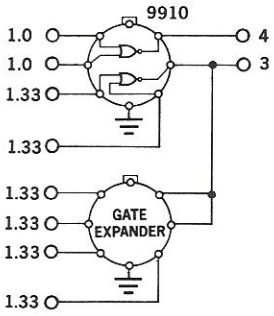
$R_1 = 1.5k\Omega$

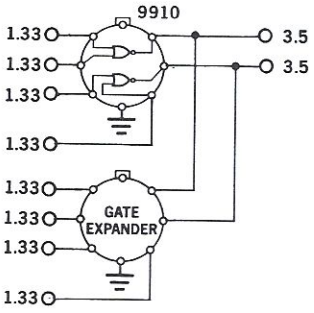
LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTORS
1	1	6	−0.5
2	1	7	−0.5
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

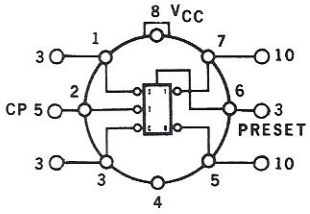
TYPICAL APPLICATIONS





9923 MEDIUM POWER JK FLIP FLOP*

The 9923 Industrial Flip-Flop is a fully integrated, monolithic circuit. This element is designed for use in industrial shift-register and binary counting applications. The 9923 JK Flip-Flop is compatible with the basic Industrial Micrologic® integrated circuit family and is guaranteed to operate at a frequency of 2.0 MHz minimum over the 0°C to 70°C temperature range.

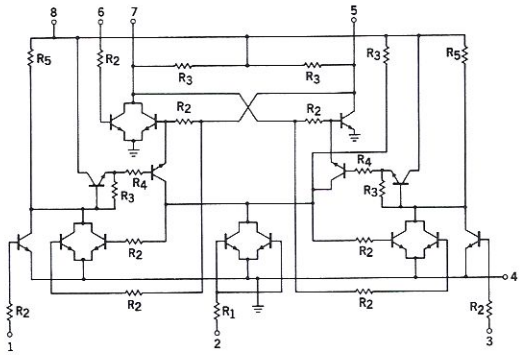


FUNCTIONS

SET (1)	CLEAR (3)	OUTPUT (7)
	$t = n$	$t = n+1$
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H = HIGH
L = LOW
X IS THE OUTPUT STATE AT TIME n
A HIGH ON PIN 6 WILL PRESET OUTPUT PIN 7 LOW

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

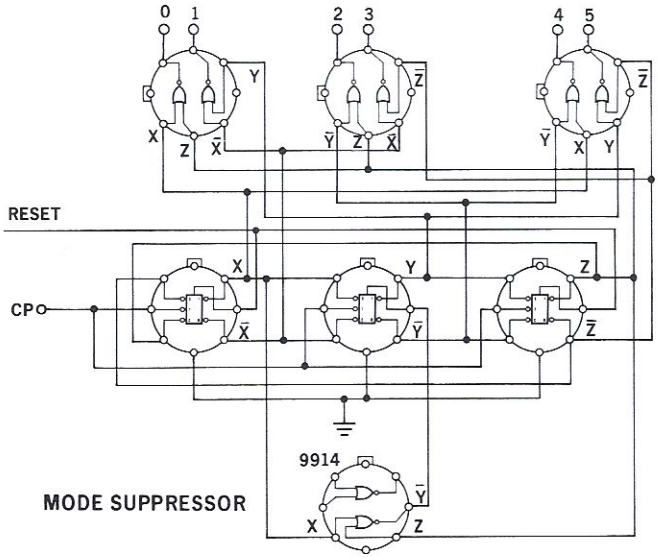
$R_1 = 260\Omega$ $R_4 = 300\Omega$
$R_2 = 450\Omega$ $R_5 = 700\Omega$
$R_3 = 640\Omega$

LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	3	5	10
2	5	6	3
3	3	7	10

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



MOD 6 SHIFT REGISTER COUNTER WITH DECODING

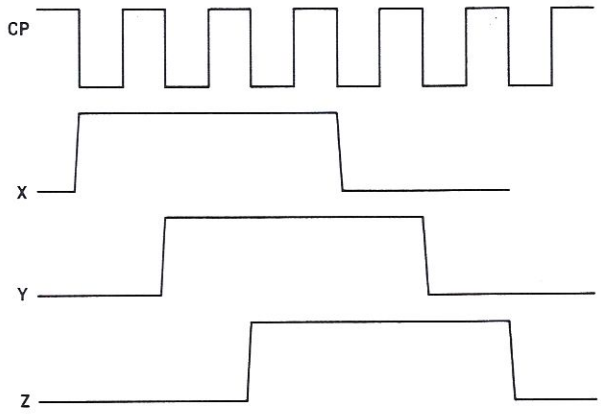
TRUTH TABLE

CT	X	Y	Z
0	L	L	L
1	H	L	L
2	H	H	L
3	H	H	H
4	L	H	H
5	L	L	H

DECODING

1	2
X	Z
$\bar{X}$	Y
$\bar{Y}$	Z
$\bar{X}$	$\bar{Z}$
X	$\bar{Y}$
Y	$\bar{Z}$

TIME DIAGRAM:



* This element also available in the epoxy package.

9926 MEDIUM POWER JK FLIP FLOP

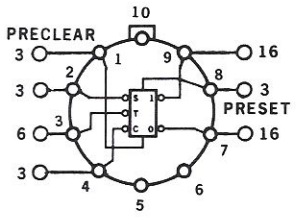
The Fairchild JK Flip-Flop is a complete, general-purpose, storage element suitable for use in shift registers, counters or any type of control function.

The JK Flip-Flop differs from ordinary RS Flip-Flops in that no ambiguous output state can result from simultaneous one inputs. In the JK Flip-Flop simultaneous ones on both the set and clear inputs cause the output state to toggle (reverse). This feature enhances the operation of the JK Flip-Flop in binary counters, as no external feedback connections are required. The toggling action can also be used to advantage for minimizing the logic structure of control units.

The unique input triggering circuit permits the JK Flip-Flop to respond to negative clock pulse transitions as short as 1 nanosecond or as long as 100 nanoseconds.

Asynchronous preset and preclear inputs are included for presetting counters, inserting parallel data in registers, and similar applications.

This element is guaranteed to operate at a frequency of 8.0 MHz minimum (20.0 MHz typical) over the 0°C to 70°C temperature range.

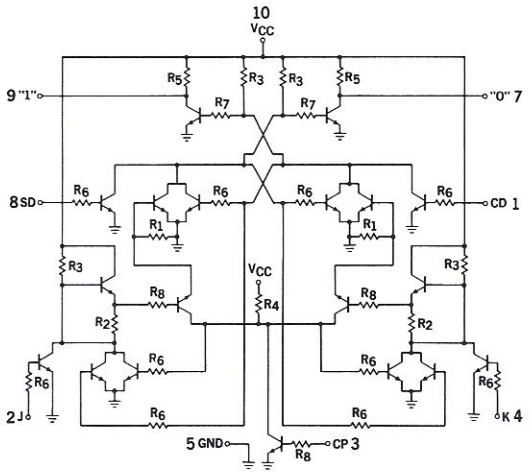


FUNCTIONS

SET (2)	CLEAR (4)	OUTPUT (9)
t = n	t = n	t = n +1
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H = HIGH
L = LOW
X IS THE OUTPUT STATE AT TIME n

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

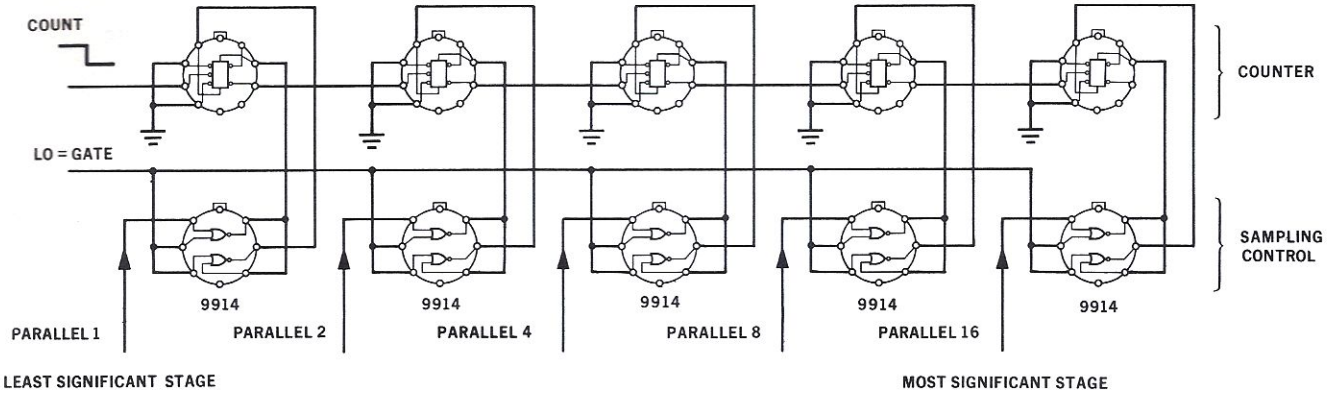
$R_1 = 3k\Omega$ $R_3 = 900\Omega$ $R_5 = 640\Omega$ $R_7 = 550\Omega$
$R_2 = 1.0k\Omega$ $R_4 = 700\Omega$ $R_6 = 600\Omega$ $R_8 = 300\Omega$

LOADING RULES

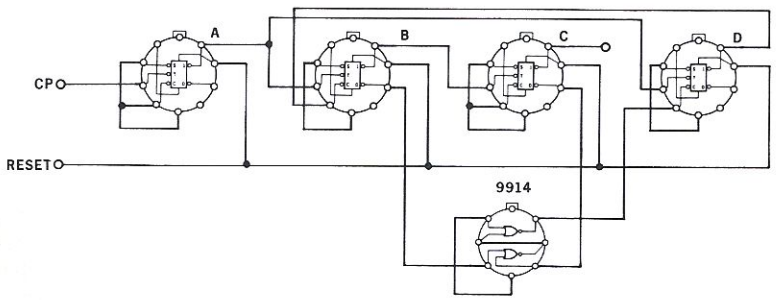
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	7	16
2	3	8	3
3	6	9	16
4	3		

Pin configurations for TO-5, Cerpak and Flatpack are identical.

TYPICAL APPLICATIONS



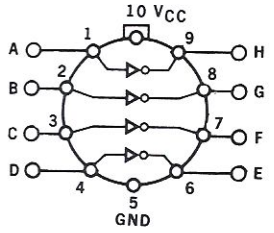
BINARY COUNTER AND SAMPLING CONTROL



1-2-4-8, MOD 10, COUNT UP COUNTER (POSITIVE LOGIC)

9927 MEDIUM POWER QUAD INVERTER

The Quad Inverter element is a four-input resistor-transistor-logic inverter circuit. This circuit is very useful where a complement of several signals is desired simultaneously.

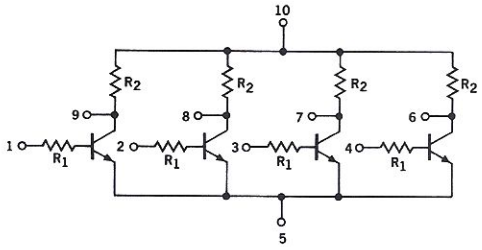


FUNCTIONS

POSITIVE AND NEGATIVE LOGIC:

$H = \overline{A}$
$G = \overline{B}$
$F = \overline{C}$
$E = \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

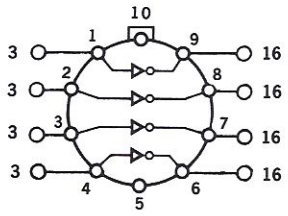
$R_1 = 450\Omega$
$R_2 = 640\Omega$

LOADING RULES

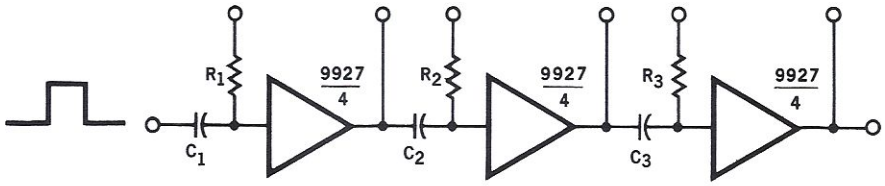
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	6	16
2	3	7	16
3	3	8	16
4	3	9	16

Note:
For more information on loading rules and for parallel combination of elements, see page 2.

LOADING CHART



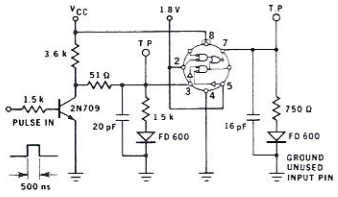
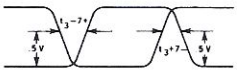
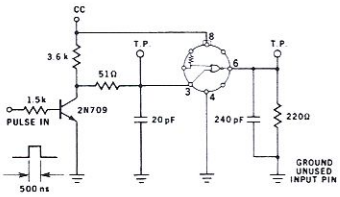
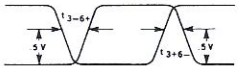
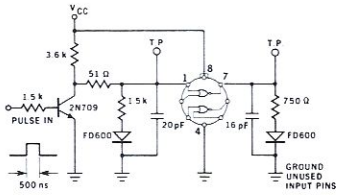
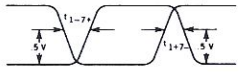
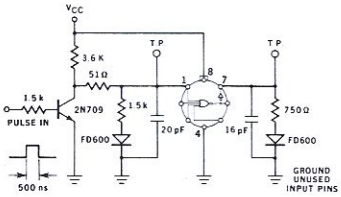
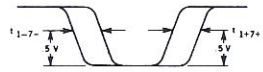
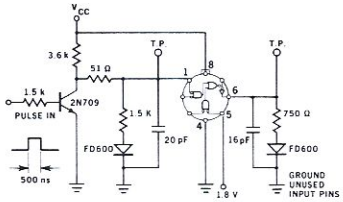
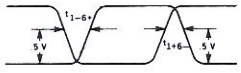
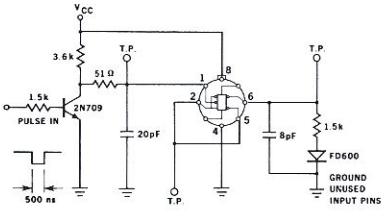
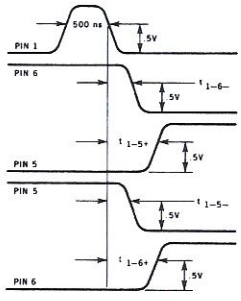
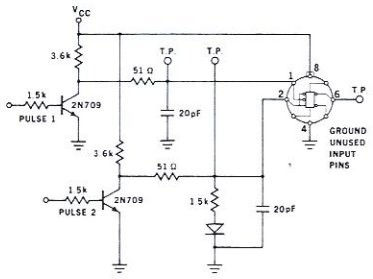
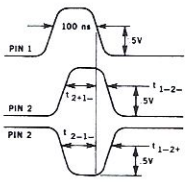
TYPICAL APPLICATIONS



DELAY INTRODUCED IN EACH STAGE IS A FUNCTION OF RC TIME CONSTANT

PULSE DELAY/SHAPER CIRCUIT

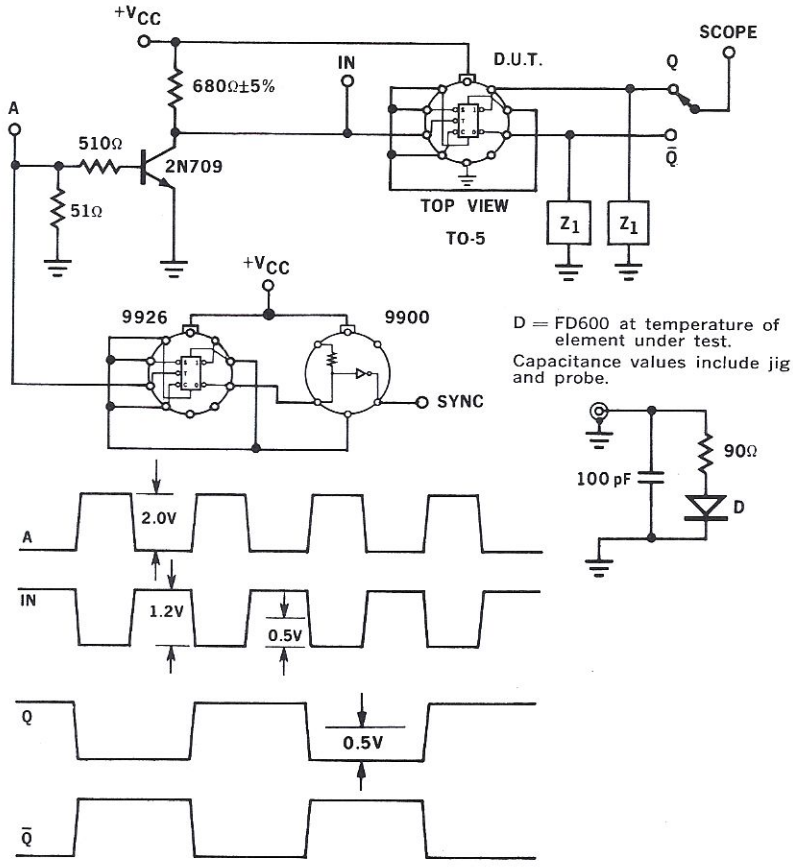
LOW POWER ELEMENTS -- PROPAGATION DELAY GUARANTEED LIMITS

ELEMENT		ns(max)		
9908	t_{3-7+} t_{3+7-}	80 100		
9909	t_{3+6-} t_{3-6+}	90 70		
9910	t_{1-7+} t_{1+7-}	40 50		
9911	t_{1-7-} t_{1+7+}	70 90		
9912	t_{1+6-} t_{1-6+}	100 80		
9913	t_{1-5-}, t_{1-6-} t_{1-5+}, t_{1-6+}	80 120		
	t_{2+1-}, t_{1-2+} t_{1-2-}, t_{2-1-}	60 min 30 min		

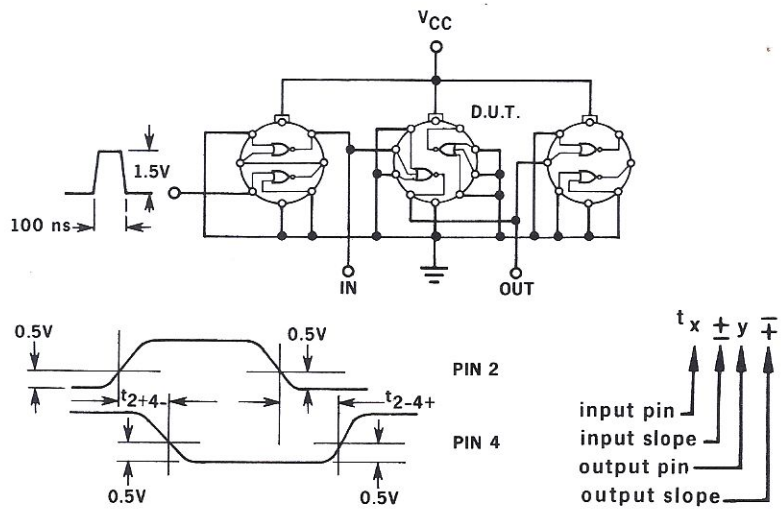
MEDIUM POWER ELEMENTS -- PROPAGATION DELAY GUARANTEED LIMITS

ELEMENT		MAX.
9900	t_{3-5-}	32 ns
	t_{3+5-}	32 ns
9903	t_{2+6-}	20 ns
	t_{2-6+}	32 ns
9905	t_{2+6-}	30 ns
	t_{2-6+}	26 ns
	t_{1+7+}	42 ns
	t_{1-7-}	42 ns
9904	t_{3+6-}	20 ns
	t_{3-6+}	32 ns
	t_{1+7+}	38 ns
	t_{1-7-}	38 ns
9907	t_{2+6-}	20 ns
	t_{2-6+}	32 ns
9914	t_{1+7-}	20 ns
	t_{1-7+}	32 ns
9915	t_{2+4-}	20 ns
	t_{2-4+}	32 ns
9923	t_{2-7+}	80 ns
	t_{2-7-}	50 ns
	t_{2-5+}	80 ns
	t_{2-5-}	50 ns
9926	t_{3-9+}	60 ns
	t_{3-9-}	60 ns
	t_{3-7+}	60 ns
	t_{3-7-}	60 ns
9927	t_{2+8-}	20 ns
	t_{2-8+}	32 ns

PROPAGATION DELAY AND TOGGLE TEST CIRCUIT FOR JK 9923 OR 9926



SWITCHING TIME TEST CIRCUIT: (FOR A GATE TYPE DEVICE)



Switching time test circuit shown above is for μL 9915, but the input and output loading circuit shown is the same for Micrologic 9900, 9903, 9904, 9905, 9907, 9914, and 9927 elements. By appropriately connecting the input and output pins of the device under test (D.U.T.) in the circuit above, switching speeds could be measured in any of the said elements.

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.